AMENDMENTS IN THE CLAIMS

1. (currently amended) A data processing system comprising:

a first processor with [[a]] first operational characteristics on a system planar;

interconnection means for later connecting a second processor on said system planar, wherein, when said second processor is heterogenous to said first processor, said interconnection means enables said first processor and said second, heterogenous processor to collectively operate as a symmetric multiprocessor (SMP) system; and

an enhanced operating system (OS) that supports inter-processing operations between said first processor and said second processor including cache coherency operations based on a collective memory configuration of the SMP, wherein said OS logs operating characteristics and cache topology data of each processor connected to the interconnection means to calculate a most efficient work allocation among processors;

wherein said interconnection means and said enhanced operating system support backward ~~and forward~~ compatibility ~~amongst~~ between said ~~first processor and said~~ second, heterogenous processor and said first processor and provides system centric enhancements for inter-processor operations including cache intervention, prefetching, and intelligent cache states.

2. (currently amended) The data processing system of Claim 1, further comprising the [[a]] second, heterogenous processor connected to said system bus via said interconnect means, wherein said second, heterogenous processor includes different physical component parameters and operational characteristics than said first processor, wherein said different physical component parameters include one or more of a higher number of cache levels, larger cache sizes, improved cache hierarchy, cache intervention, and larger number of on-chip processors.

3. (currently amended) The data processing system of Claim 1, further comprising a cache coherency protocol that supports non-homogenous cache configurations amongst heterogenous processors, said non-homogenous cache configurations including one or more of:

a first cache of the first processor [[begin]] being designed to support a first set of cache/memory operations with an associated first set of coherency states while a second cache of

the second processor is designed to support a similar set of memory operations with additional coherency states;

[[said]] a second cache supporting cache intervention from similarly configured caches;

different levels of caches, cache states, and shared caches among processors;

different cache sizes and cache line widths, wherein a first cache line of the first processor's cache ~~having~~ has a different width from a cache line of the second processors cache.

4. (currently amended) The data processing system of Claim 3, wherein said interconnect means is coupled to a system bus and comprises a plurality of buses for connecting additional processors to said system bus, said buses comprising a system data bus, base address bus, master processor select bus, base snoop response bus, and extended snoop response bus, wherein each bus includes one or more pins ~~that are set/reset to indicate a particular condition of a connected component~~.

5. (currently amended) The data processing system of Claim 4, wherein said master processor select bus includes a first set of pins, each connected to an added processor, wherein when one of said first set of pins is set to an active state, the connected processor operates as a master on the master processor select bus.

6. (currently amended) The data processing system of Claim 5, wherein:

a respective pin is set when a read operation is issued to ~~indicating~~ indicate that the issuing processor is the master processor; and

when said read operation is snooped by a second added processor with a cache line in the R coherency state, the second added processor drives the extended snoop response bus with shared intervention information and sends a retry response on the base snoop response bus.

7. (currently amended) The data processing system of Claim 6, wherein said operational characteristics of each processor connected to the interconnection means include[[s]] one or more of:

operating frequency, wherein the second processor operates at a higher frequency than said first processor ; and

an instruction ordering mechanism, wherein said first processor and second processor utilize[[s]] a different one of a plurality of instruction ordering mechanisms from among in-order processing, out-of-order processing, and robust out-of-order processing.

8. (previously presented)The data processing system of Claim 3, wherein all caches are sectored into widths representing a smallest width cache line that is accessible within the overall data processing system.

9. (previously presented)The data processing system of Claim 1, further comprising a switch that provides direct point-to-point connection between said first processor and later added processors.

10. (currently amended) A method for upgrading processing capabilities of a data processing system comprising:

providing a plurality of interrupt pins from a system bus on a system planar to allow later addition of other processors;

enabling direct connection by a heterogenous processor to said system planar via said plurality of interrupt pins, wherein said plurality of interrupt pins provide communication paths between said heterogenous processor and other processors previously attached to said system planar; and

providing support for full backward compatibility by said [[new,]] heterogenous processor when said [[new]] heterogenous processor comprises more advanced operational characteristics to enable said data processing system to operate as a symmetric multiprocessor system (SMP), wherein said support includes an enhanced operating system (OS) that supports inter-processing operations between said [[first]] heterogenous processor and said ~~second~~ other processors including cache coherency operations based on a collective memory configuration of the SMP, wherein said OS logs operating characteristics and cache topology data of each processor connected to the ~~interconnection means~~ system bus to calculate a most efficient work allocation among processors;

wherein said interconnection means and said enhanced operating system support backward ~~and forward~~ compatibility ~~amongst~~ between said ~~first processor and said second~~,

heterogenous processor and said other processors and provide[[s]] system centric enhancements for inter-processor operations including cache intervention, pre-fetching, and intelligent cache states.

11. (currently amended) The method of Claim [[7]] 10, wherein said interconnect means is coupled to a system bus and comprises a plurality of buses for connecting additional processors to said system bus, said buses comprising a system data bus, base address bus, master processor select bus, base snoop response bus, and extended snoop response bus, wherein each bus includes one or more pins that are set/reset to indicate a particular condition of a connected component;

wherein said master processor select bus includes a first set of pins, each connected to an added processor, wherein one of said first set of pins is set to an active state when the connected processor operates as a master on the master processor select bus;

wherein when said one pin is set when a read operation is issued to ~~indicating~~ indicate that the issuing processor is the master processor; and

when said read operation is snooped by a second added processor in the R coherency state, the second added processor drives the extended snoop response bus with shared intervention information and sends a retry response [[to]] on the base snoop response bus.

12. (currently amended) A multiprocessor system comprising:

a plurality of heterogenous processors with different operational characteristics and physical topology connected on a system planar;

a system bus that supports system centric operations;

interrupt pins coupled to said system bus that provide connection for at least one of said plurality of heterogenous processors;

an enhanced system bus protocol that supports downward compatibility of a newer processor[[s]] that is designed with advanced operational characteristics from among said plurality of heterogenous processors to a first processor[[s]] that does not support said advance operation characteristics;

an enhanced operating system (OS) that supports inter-processing operations between said first processor and said ~~second~~ newer processor including cache coherency operations based

on a collective memory configuration of the SMP, wherein said OS logs operating characteristics and cache topology data of each processor connected to the system bus ~~interconnection means~~ to calculate a most efficient work allocation among processors;

wherein said enhanced system bus protocol and said enhanced operating system support backward ~~and forward~~ compatibility ~~amongst~~ between said ~~first processor and said~~ second, heterogenous processor and said first processor and provide[[s]] system centric enhancements for inter-processor operations including cache intervention, prefetching, and intelligent cache states.

13. (currently amended) The multiprocessor system of Claim 12, further comprising a switch that provides direct point-to-point connection between each of said plurality of heterogeneous processors and later added processors.

14. (currently amended) The multiprocessor system of Claim 12, wherein said plurality of heterogeneous processors includes heterogenous processor topologies including different cache sizes, cache states, number of cache levels, and number of processors on a single processor chip.

15. (currently amended) The multiprocessor system of Claim 13, further comprising a cache coherency protocol that supports non-homogenous cache configurations amongst heterogenous processors, said non-homogenous cache configurations including one or more of:

a first cache of [[the]] a first processor being designed to support a first set of cache/memory operations with an associated first set of coherency states while a second cache of [[the]] a second processor is designed to support a similar set of memory operations with additional coherency states;

[[said]] a second cache supporting cache intervention from similarly configured caches;

different levels of caches, cache states, and shared caches among processors;

different cache sizes and widths of cache lines, wherein a first cache line of the first processor's cache ~~having~~ has a different width from a cache line of the second processor's cache.

16. (previously presented)The multiprocessor system of Claim 15, wherein all caches are sectored into widths representing a smallest width cache line that is accessible within the overall data processing system.

17. (previously presented)The multiprocessor system of Claim 15, wherein said ~~interconnect means is coupled to a~~ system bus [[and]] comprises a plurality of buses for connecting additional processors to said system bus, said plurality of buses comprising a system data bus, base address bus, master processor select bus, base snoop response bus, and extended snoop response bus, wherein each bus includes one or more pins ~~that are set/reset to indicate a particular condition of a connected component~~.

18. (previously presented)The multiprocessor system of Claim 17, wherein said master processor select bus includes a first set of pins, each connected to an added processor, wherein when one of said first set of pins is set to an active state, the connected processor operates as a master on the master processor select bus.

19. (previously presented)The multiprocessor system of Claim 18, wherein:

the ~~respective~~ one of the first set of pins is set when a read operation is issued to ~~indicating~~ indicate that the issuing processor is the master processor; and

when said read operation is snooped by a second added processor with a cache line in the R coherency state, the second added processor drives the extended snoop response bus with shared intervention information and sends a retry response on the base snoop response bus.

20. (previously presented)The multiprocessor system of Claim 19, wherein said operational characteristics of each processor connected to the system bus include[[s]] one or more of:

operating frequency, wherein the second added processor operates at a higher frequency than said first processor; and

an instruction ordering mechanism, wherein said first processor and second added processor utilizes a different one of a plurality of instruction ordering mechanisms from among in-order processing, out-of-order processing, and robust out-of-order processing.